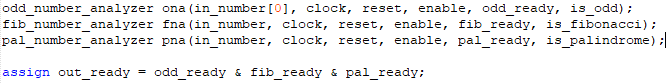
CSE 433 Project 2 - FSM Number Analyzer

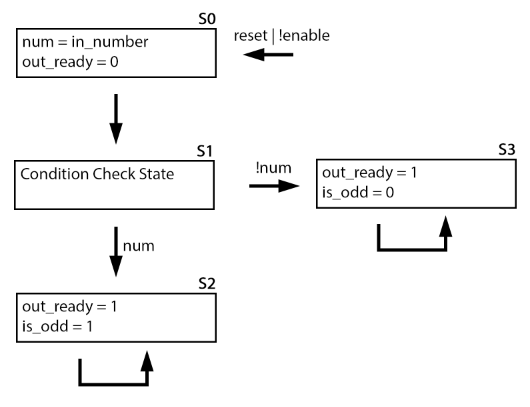
# Finite State Machine

To simplify design process, I designed 3 properties of number analyzer as 3 different finite state machines. After implemented 3 separate machines as Verilog modules, I then simply wired all three together in Number Analyzer module.

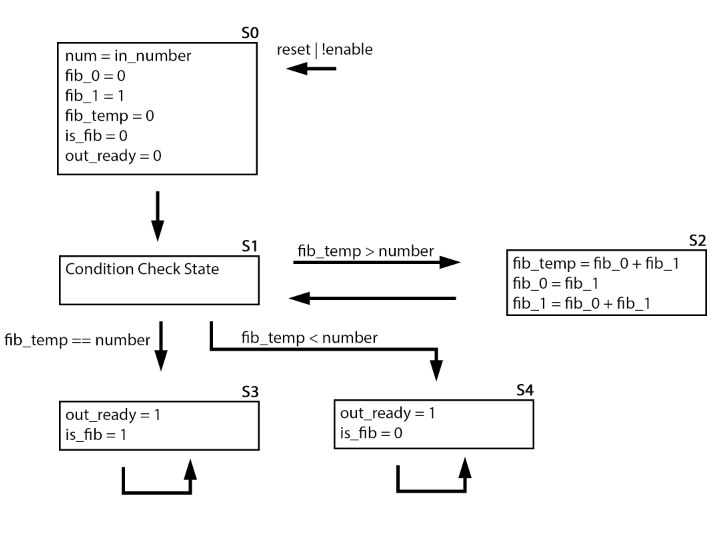


From all states in all modules, reset signal can trigger next state as S0. Also if enable signal is not high, fsm will always stay at S0.

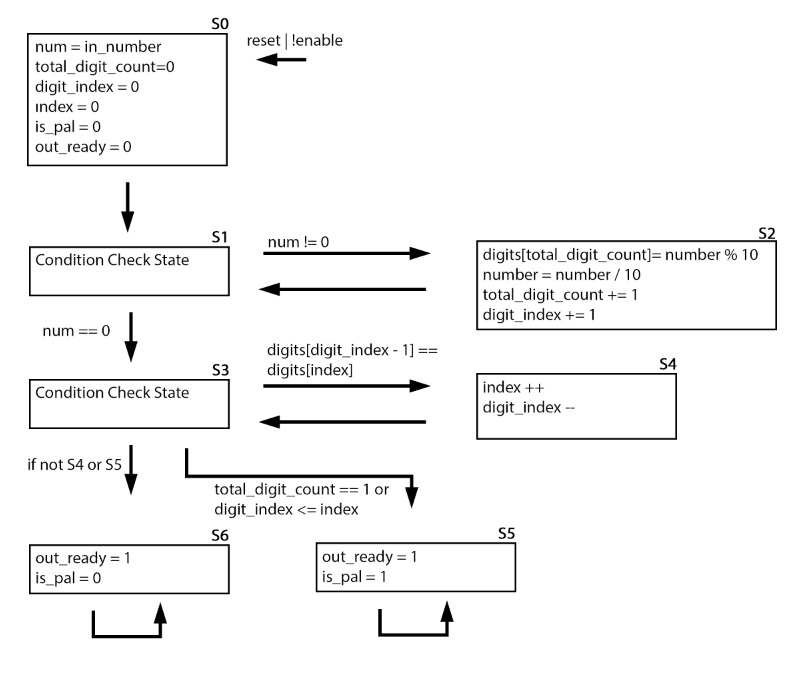
## Odd Number Analyzer State Diagram



## Fibonacci Number Analyzer



## Palindrome Number Analyzer



# Simulation Results

Testbench has an array of 32 bit numbers. It starts with number 0 and tests all test values whenever number analyzer sends an outputs ready signal. It sends reset signal alongside with each new value to reset number analyzer module. Array size can be changed to support more values to test in a single run.

We can see different modules outputs in different times. For example for number 1345269, is odd output is really fast but is Fibonacci result comes much later. And once it is ready, all outputs are ready signal is received from the top level module. Last column shows that if all three results are ready or not.

